Remarks

Claims 1-11, 15-17 and 41-68 are pending.

The Examiner rejected Claims 1-11 and 15-17 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 6,018,178 ("Sung"), in view of U.S. Patent 5,760,435. With respect to independent Claim 1, the Examiner cites as the reason to combine the references:

> ... Thus, Sung is shown to teach all the features of the claim with the exception of explicitly disclosing the third height is higher than the first and second heights.
>
> However, Pan teaches an electrically alterable memory device having a control gate (30), first (61) and second (62) floating gates formed on a semiconductor substrate (10), wherein the control gate (30) has a third height that is higher than both first (61) and second (62) floating gates. (See Fig. 10).
>
> Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the control gate of the electrically alterable memory device of Sung higher than the first and second floating gates as taught by Pan to double storage efficiency.

Applicants respectfully submit that the Examiner's rejection is invalid because the prior art provides no suggestion or motivation to modify the teachings of Sung in the manner suggested by the Examiner. Thus, pursuant to the requirements of MPEP § 2143.01(I), the Examiner failed to set forth a *prima facie* case of obviousness. The Examiner's rejection fails because (i) the modification suggested by the Examiner is unrelated the Examiner's motivation "to achieving double storage efficiency," and (ii) Sung already achieves double storage efficiency without the modification suggested by the Examiner.

The Examiner cites as the reason Pan's objective is to provide "a high density memory cell with one control gate and two floating gates of doubled storage efficiency ..."

(Pan, at col. 3, lines 38-42). To meet the limitations of Applicants' Claim 1 (i.e., the height of the control gate exceeds those of the floating gates), the Examiner refers to Pan's Fig. 10, where an etching has removed a capping oxide layer 55 and sufficient sidewall spacers 61 and 62, so that the exposed height of control gate 30 is greater than the heights of the sidewall spacers 61 and 62. However, at col. 5, lines 36-47, Pan clearly teaches that the modification suggested by the Examiner is unnecessary for achieving its objective of double storage efficiency:

> The second layer of polysilicon (60) of FIG. 7 is deposited to a thickness of between about 2,000 to 4,000 Å over the substrate shown in FIG. 7 and then etched back to form the wide spacers 60' shown in FIG. 8. ... It will be noted in FIG. 8 that the PolySi (60) of FIG. 7 has been over-etched to remove the top oxide layer (55) of the latter Fig.. Although this is the preferred mode, it is not necessary.
>
> (emphasis added)

Therefore, the Examiner's reason for modifying Sung's teachings is invalid, as Pan clearly shows that the Examiner's suggested modification of Sung is irrelevant to the goal of achieving double storage efficiency.

Further, as discussed in Sung's col. 2, lines 11-14, Sung itself already discloses a memory cell that offers multiple data storage:

> In accordance with the present invention a process for creating an EEPROM cell, offering multiple data storage, on the same cell, and floating gate spacer structures, for density improvements, is described.

Thus, there is no reason to make the Examiner's suggested modification of Sung's teachings in the direction of Pan. Therefore, nothing in the prior art suggests or motivates the Examiner's proposed modification of Sung's teachings in view of Pan. Accordingly,

Applicants respectfully submit that Claim 1 and its dependent Claims 2-11 and 15-17 are allowable over the combined teachings of Sung and Pan. Reconsideration and allowance of these claims are therefore requested.

The Examiner rejected Claims 41-48, 50 and 52-54 under 35 U.S.C. § 103(a) as being unpatentable over Sung, in view of U.S. Patent 6,271,089 ("Chen"). With respect to independent Claim 41, to support the Examiner's proposed modification of Sung's teachings, in the direction of Chen, the Examiner states:

> ... Thus, Sung is shown to teach all the features of the claim with the exception of explicitly disclosing the control gate covering the first and second floating gate on at least right side and left side.
>
> However, Chen teaches the control gate (208) of electrically. alterable memory device covering the first (204a) and second (204b) floating gate on at least right side and left side. (See Fig. 2B).
>
> Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the control gate of the electrically alterable memory device of Sung to cover the first and second floating gates on at least right side and left side as taught by Chen to increase the numbers of bits stored in the unit area of a flash memory.

Applicants respectfully traverse the Examiner's rejection. As discussed in Chen's col. 3, lines 52-54, Chen clearly states that it owes its increase in number of bits stored per unit area to the number of floating gates per memory cell, and not to coverage by the control gate on the floating gates:

> Because each of the floating gates 204a and 204b can store one bit, the numbers of bits stored in the unit area is increased.

Thus, as in Pan (discussed above), the Examiner's reason for modifying Sung's

teachings is invalid, as Chen clearly shows that there is no desirability for making the Examiner's suggested modification of Sung. The Examiner's proposed modification is simply irrelevant to the Examiner's proposed motivation or suggestion. Further, as discussed above, Sung itself also already discloses a memory cell that offers multiple data storage. Thus, there is no reason to make the Examiner's suggested modification of Sung's teachings in the direction of Chen. Therefore, nothing in the prior art suggests or motivates the Examiner's modification of Sung's teachings in view of Chen. The Examiner's rejection thus failed to set forth a *prima facie* case of obviousness, as required by MPEP § 2143.01(I). Claims 42-48, 50 and 52-54 are therefore allowable over the combined teachings of Sung and Chen. Reconsideration and allowance of Claim 41 and its dependent Claims 42-48, 50 and 52-54 are requested.

The Examiner rejected Claims 49 and 51 under 35 U.S.C. § 103(a) as being unpatentable over Sung and Chen, as applied to Claim 41, and further in view of Pan. As Claims 49 and 51 each depend from Claim 41, Claims 41 and 59 are each allowable over the combined teachings of Sung and Chen because of the deficiency in the Examiner's combination of Sung's and Chen's teachings, as discussed above. As the Examiner merely cites Pan for teaching using ONO as an insulator material, the combined teachings of Sung, Chen and Pan neither disclose nor suggest Applicants' Claims 49 and 51. Reconsideration and allowance of Claims 49 and 51 are therefore requested.

The Examiner rejected Claims 55-68 under 35 U.S.C. § 103(a) as being unpatentable over Sung, in view of U.S. Patent 5,576,232 ("Hong"). The Examiner cites as the reason for modifying Sung's teachings in the direction of Hong as follows:

> Thus, Sung is shown to teach all the features of the claim with the exception of explicitly disclosing the control gate being covered by the first and second floating gates on more than one lateral side.

> However, Hong teaches the control gate (520) of the electrically alterable memory device being covered by the first floating gate (580) and second floating gate (580) on more than one lateral side. (See Fig. 7H).
>
> Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the control gate of the electrically alterable memory device of Sung being covered on more than one lateral side by the first and second floating gates as taught by Hong to improve device reliability.

Applicants respectfully traverse the Examiner's rejection. Contrary to the Examiner's assertion, Hong does not teach the control gate covering a first floating gate and a second floating gate, as Hong's sidewall spacers constitute only a single floating gate:

> Referring next to FIG. 7h, an etching procedure employing, for example, plasma etching, is conducted to etch away all of conducting layer 58 except those portions forming sidewall spacers 580 covering conducting strips 540, as well as the sidewalls of isolating oxide layers 570 on both sides. Each of sidewall spacers 580, being a conductor itself also cover the area of tunnel oxide layer 57 near the generally vertical sidewall of isolating oxide layers 570, as well as the exposed edges of gate dielectric layer 53, while being isolated from control gate 520. Conducting strips 540 and sidewall spacers 580, being directly and electric-conductingly connected to each other, together constitute the floating gate of the memory cells of the flash memory device.
>
> (emphasis added)

The modification that the Examiner's suggests to make to improve device reliability would therefore reduce the number of data bits stored in the memory cell to one. Sung, however, has as its stated objective "to create an EEPROM cell offering multiple storage levels" (Sung, at col. 2, lines 6-7). Thus, the Examiner's proposed modification of Sung would render Sung's device to be unsatisfactory to -- indeed, frustrates -- Sung's stated purpose. MPEP § 2143.01 states that such a result mandates the conclusion that the prior art

neither suggests nor motivates the Examiner's modification:

> If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984)

Accordingly, Applicants respectfully submit that the Claims 55-68 are each allowable over the combined teachings of Sung and Hong. Reconsideration and allowance of Claims 55-68 are therefore requested.

Therefore, for the reasons set forth above, all pending claims (i.e., Claims 1-11, 15-17 and 41-68) are allowable over the art of record. If the Examiner has any question regarding the above, the Examiner is respectfully requested to telephone the undersigned Attorney for Applicant at 408-392-9250.

Certificate of Transmission: I hereby certify that this correspondence is being transmitted to the United States Patent and Trademark Office (USPTO) via the USPTO's electronic filing system on February 6, 2007.

Attorney for Applicant(s) — Date of Signature: 2/6/2007

Respectfully submitted,

Edward C. Kwok
Attorney for Applicant(s)
Reg. No. 33,938

Law Offices of
MacPherson Kwok Chen & Heid LLP
2033 Gateway Place, Suite 400
San Jose, CA 95110
Tel: (408) 392-9250
Fax: (408) 392-9262